PATENT ABSTRACTS OF JAPAN

(11)Publication number : 　　　　2000-029685

(43)Date of publication of application : 28.01.2000

---

(51)Int.Cl.

G06F 9/30
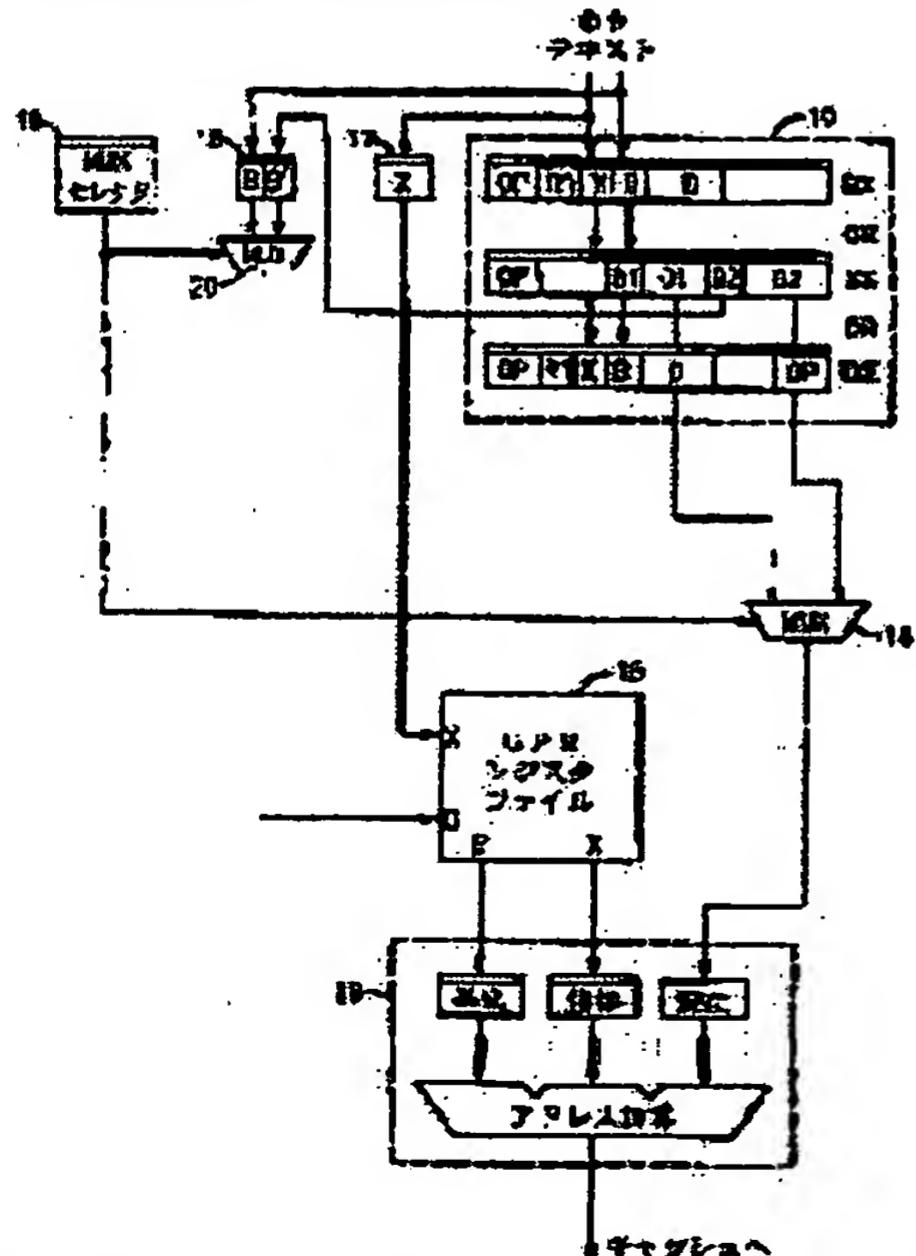G06F 9/355
G06F 9/38

---

(54) COMPUTER SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To enable a foating-point processor to determine the accurate format of an instruction by determining that an instruction is in 2nd format by decoding an operation code and gating information needed for address generation to an adder according to the decision result.

SOLUTION: A 2nd base register is gated from an instruction text to a B prime slot in a base register 18 in a 1st cycle and a multiplexer selector 19 is set to 1. A critical path, therefore, reaches a register for an address adder 16 from the base register 18 through a multiplexer 20 controlled by the selector 19 and a GPR file 15. In this case, the floating-point processor decodes a 1st part of the operation code to determine that the instruction is in 2nd format, and gates information needed for address generation to the adder 16 according to the determination result.